ABSTRACT OF THE DISCLOSURE

A buffer circuit is provided having a driver device and an input device to receive a first set of signals and to produce a second set of signals. The driver device may receive the second set of signals and output a third set of signals based on the second set of signals input to said driver device. A comparing device may receive the third set of signals from the driver device and produce a fourth set of signals based on the third set of signals, the comparing device may compare the fourth set of signals with the first set of signals.